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PATENT
8001-1176

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Atsushi KUWATA

Conf. 4322

Application No. 10/720,162

Group 2182

Filed November 25, 2003

Examiner Scott C. Sun

DISK ARRAY APPARATUS AND DATA WRITING METHOD
USED IN THE DISK ARRAY APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed Form PTO-1449.

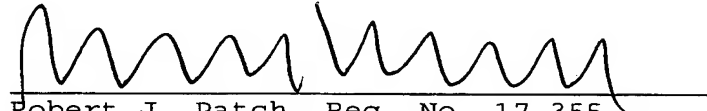
A concise explanation of the relevance of these items is that these references were cited by the Japanese Patent Office in the corresponding Japanese Application Serial No. 2003-001314, filed January 7, 2003. A copy of the Japanese Official Action in which they were cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. **An English translation of the enclosed portion is also attached hereto.**

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information contained in this Information Disclosure Statement was first

cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Statement.

Respectfully submitted,

YOUNG & THOMPSON

A handwritten signature in black ink, appearing to read 'Robert J. Patch', is written over a horizontal line.

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U. S. Application No. 10/720,162

Our Ref. 8001-1176

a) Claims 1 and 6

In section [0045] and [0048] of Citation 1, reference is made to the essence of accomplishing a clean state wherein, relative to the renewal of data from a data processing device, a storage control device stores new data in cache memory, creates parity relative to the data, and by turning a physical dirty flag ON relative to a segment storing new data, accomplishes a physically dirty state in which the created new parity also is made to be the dirty state, and when the data and parity complete reflection to the disk device, a clean state is achieved by turning the physically dirty flag OFF.

With the invention relating to Claims 1 and 6 of the present invention (hereafter referred to as "present application inventions 1-6"), attached data which relates to a logical address is stored in cache memory, attached in relation to a physical address. However, with the invention recorded in Citation 1 (hereafter referred to as a "Citation invention 1", there is a difference in the point that the subject composition is unclear.

However, as recorded in Figure 4 of Citation 2, recording data which is stored in cache memory to a logical address and physical address would be known technology to one skilled in the art.

Furthermore, inventions 1-6 of the present application could be easily obtained by one skilled in the art by applying known technology to Citation 1

Moreover, since providing multiple control units and using non-volatile memory as the cache memory would be known technology in the subject technology sector, it could be appropriately obtained by one skilled in the art.

Reference Citation List

1. Japanese Unexamined Patent Application H10-312246
2. Japanese Unexamined Patent Application H07-152499

Record of the Examination Results relating to Documents of the
Prior Art

- Examined Technical Field: IPC 7th Edition G06F 3/06

The record of the examination results relating to documents of the prior art does not constitute the grounds for rejection.

(Use several sheets if necessary)

Group Art Unit:
2182

[illegible][illegible]

DATE CONSIDERED

* Abstract provided for the Examiner's convenience